IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	§	**Group Art Unit: 2182**
Hofstee, et. al.	§	
	§	**Examiner: Hassan, Aurangzeb**
Serial No.: 10/697,903	§	
	§	**Attorney Docket No.**
Filed: October 30, 2003	§	**AUS920030403US1**
	§	
Title: System and Method for a Configurable Interface Controller	§	**IBM Corporation**
	§	**Intellectual Property Law Dept.**
	§	**11400 Burnet Road**
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APPELLANTS' REPLY BRIEF (37 CFR 1.193)

Sir:

A. INTRODUCTORY COMMENTS

Appellants now present this Reply Brief in response to the Examiner's Answer of February 6, 2008, and make the following responses to the Examiner's arguments. Appellants' Reply Brief responds to several of the arguments made by the Examiner in the Examiner's Answer. For a full discussion of Appellants' arguments, see Appellants' Appeal Brief, filed on November 13, 2007.

No extension of time is believed to be necessary. If, however, an extension of time is required, the extension is requested, and the undersigned hereby authorizes the Commissioner to charge any fees for this extension to IBM Corporation Deposit Account No. 09-0447.

B. ARGUMENTS

Appellants Claims are Allowable over Matsushita in view of Miller.

Response to First Examiner's Response (see Answer, page 7, para. starting on line 9)

The Examiner's Answer continues to maintain that "Matsushita discloses the I/O controller connected to multiple I/O devices but does not specifically disclose a system having plurality of interface controllers; a means for selecting the first interface controller from the plurality of interface controllers that correspond to the first assignment request" (see Examiner's Answer, page 4, paragraph starting on line 9). As Appellants have repeatedly and fervently argued, Matsushita ***simply does not teach the use of a plurality of I/O controllers***. The Examiner has repeatedly pointed to Matsushita's elements numbered 104, 106, and 108 as being such "I/O controllers." However, a simple viewing of the Matsushita reference reveals that elements 104, 106, and 108 are ***multiplexers***, and are ***NOT*** I/O controllers.

In response to Appellants' argument that Matsushita does not teach the subject matter asserted by the Examiner, the Examiner responds that "... one cannot show nonobviousness by attacking individually where the rejections are based on combinations of references" (citations omitted). Appellants respond that MPEP § 2144.06 allows art to be used when there is a recognized equivalence for the same purpose, however, here the Examiner has not shown that Matsushita's multiplexers are equivalent to the I/O controllers that they are being used to reject. Indeed, MPEP § 2144.06(I) allows "combining equivalents known for the same purpose, while MPEP § 2144.06(II) allows "substituting equivalents known for the same purpose." Here, the Examiner wishes to substitute Appellants' "I/O controllers" with Matsushita's "multiplexers" even though multiplexers and I/O controllers are simply not interchangeable nor are these devices known for the same purpose. Taking the Examiner's response to the extreme, the Examiner could just as easily have found a reference that selected an orange from a plurality of oranges and then argued that the "orange" reference taught the "selecting" and the Miller reference taught the I/O controllers even though oranges and I/O controllers are not equivalent or interchangeable, just as multiplexers and I/O controllers are not equivalent or interchangeable.

Then, as here, when Appellants pointed out the absurdity of using the "oranges" reference, the examiner could broadly dismiss Appellants' argument as "attacking references individually."

MPEP § 2144.07, entitled "Art Recognized Suitability for an Intended Purpose" also lends weight to Appellants' arguments. *In re Leshin*, cited in § 2144.07, dealt with the obviousness of a bagging machine where the difference between the claimed invention and the prior art was that one had a hydraulic brake whereas the other had a mechanical brake. *In re Leshin* is not analogous to Appellants' claims because a "multiplexer" is not a suitable alternative to an "I/O controller" and does not serve the same intended purpose. The multiplexer selects one of a plurality of signals, where, in contrast, an I/O controller operates to control communication between a device and a peripheral. For example, if a design required a module to communicate with a peripheral device, an I/O controller module could be used, however one could not substitute a multiplexer to perform the same intended purpose.

Moreover, Appellants' disagree that they have attacked the references individually. The Examiner used the references individually as purportedly teaching various limitations of Appellants' claimed invention. Appellants have merely pointed out that one of the references (Matsushita) ***does not teach*** what the Examiner purports. The Examiner should not be able to purport that a reference, such as Matsushita, teaches a particular limitation and then, when Appellants question this assertion, hide the fact of the reference's failing by attacking the Appellant as "attacking an individual reference."

Response to Second Examiner's Response (see Answer, page 8, para. starting on line 6)

Moving to Appellants' next argument, the Examiner's Answer points out that Appellants argue:

> The Final Office Action contends that Matsushita teaches Applicant's claimed limitation of "selecting a first interface controller from a plurality of interface controllers that correspond to the first assignment request," citing Matsushita's multiplexers (104, 106, and 108). While multiplexers are used for selecting data, the multiplexers used by Matsushita do not teach anything regarding selecting an "interface controller from a plurality of interface controllers," as claimed by Applicant. Instead, Matsushita uses the multiplexers to either replace an address signal (46) with output data (120), or leave the addresses unchanged (Matsushita, col. 6, lines 36-57). In this manner, Matsushita teaches that different

semiconductor devices can be tested by replacing the pin assignment data in the pin map memory (col. 6, line 58 – col. 7, line 4).

In response to Appellants' argument, on page 8, middle of the page, the Examiner's Answer responds that "the Examiner has cited Matsushita's multiplexers (104, 106, and 108) for selection purposes, however such citation was not included in the latest Office Action sent out on 7/5/2006." Appellants are quite puzzled by the Examiner's response. Not only in the Final Office Action of 7/5/2006 (paragraph starting on page 3, line 7), but even in the Examiner's Answer (paragraph starting on page 4, line 11), the Examiner states (emphasis added):

"Matsushita discloses the I/O controller connected to multiple I/O devices but does not explicitly disclose a system having a plurality of interface controllers; ***a means for selecting a first interface controller from the plurality of the interface controllers that correspond to the first assignment request.***"

Note that the Examiner does not state that Matsushita ***does not teach*** the "means for selecting..." and that the highlighted portion is in a paragraph purporting to show what Matsushita teaches. A fair reading of the Examiner's rejection is that the Examiner is asserting (1) that Matsushita teaches the I/O controller connected to multiple I/O devices (again, as Appellants point out, Matsushita does not teach an I/O controller but rather a set of multiplexers), (2) that Matsushita does not disclose a system with a plurality of interface controllers, and (3) that Matsushita teaches "a means for selecting a first interface controller from the plurality of the interface controllers that correspond to the first assignment request" (which, as Appellants' detail in the Appeal Brief, Matsushita does not teach such selection of a first interface controller from a plurality of interface controllers because Matsushita does not teach or suggest a plurality of interface controllers). If Appellants' reading of the Examiner's rejection is not as intended by the Examiner, then Appellants respectfully submit that, on its face, the rejection is confusing. It is unclear as to what the Examiner asserts as Matsushita's actual teachings versus what Matsushita is not teaching. Finally, the Examiner correctly notes that Appellants' argument in the Appeal Brief is "verbatim" the argument presented to the Examiner in the Response dated 3/30/2006, precisely because the wording of the Examiner's rejection, as described above, appears to indicate that the Examiner is relying on Matsushita as teaching the "means for selecting..." limitation and has remained unchanged.

Response to Third Examiner's Response (see Answer, page 9, para. starting on line 1)

In the Examiner's Response, the Examiner states that "wherein Matsushita teaches an interface controller associated with an I/O device but does not explicitly disclose a method in which one can be selected from a plurality of controllers which is relied upon in Miller." However, as repeatedly argued by Appellants, Matsushita does not "teach an interface controller" let alone "an interface controller associated with an I/O device." Appellants have electronically scanned the entire Matsushita reference and note that none of the words "interface," "interface controller," "I/O," "I/O device," or "input/output" are found in Matsushita. Matsushita is a patent directed at a testing system for a semiconductor device and does not teach or suggest anything to do with interface controllers and their use with I/O devices. The Examiner's continued reliance on Matsushita as teaching these limitations is outright baffling. Appellants respectfully direct the Board's attention to MPEP § 2145(X)(D)(1) entitled "The Nature of the Teaching Is Highly Relevant." Here, the Examiner's primary reference is directed at a semiconductor testing system and does not teach or suggest anything to do with I/O controllers. The lack of relevance of the primary reference (Matsushita) to Appellants' claims further buttresses Appellants' arguments that the references of Matsushita, alone or combined with the teachings of Miller, do not teach or suggest Appellants' claimed limitations and do not render Appellants' claims obvious in light of such teachings.

Response to Fourth Examiner's Response (see Answer, page 9, para. starting on line 18)

Once again, the Examiner states that "Matsushita teaches an interface controller and multiple I/O devices…" Appellants respectfully direct the Board's attention to the preceding Response that outlines that nowhere does Matsushita use any of the words "interface," "interface controller," "I/O," "I/O device," or "input/output" and so does not teach what the Examiner purports.

Again, the Examiner attempts to hide behind the failings of the cited references, in this case Matsushita, by attacking the Appellants for pointing out that a reference simply does not teach or suggest what the Examiner says it teaches. As discussed in preceding Responses, Appellants' discussion of the failure of cited art to teach what is purported by the Examiner is entirely permissible under applicable sections of the MPEP (e.g., MPEP § 2145).

Response to Fifth Examiner's Response (see Answer, page 11, para. starting on line 1)

Here the Examiner responds that "Furthermore the Examiner explicitly disclosed that Matsushita teaches an interface controller connected to multiple I/O devices but did not disclose the **selecting** algorithm from a plurality of interface controllers for which Miller was introduced as a secondary reference." (emphasis in original). However, as pointed out in the above sections, Matsushita does not teach or suggest an interface controller connected to multiple I/O devices, as repeatedly argued by the Examiner. Matsushita is **completely void** of any of the terms including "interface," "interface controller," "I/O," "I/O device," or "input/output" and so does not teach what the Examiner purports.

Response to Sixth Examiner's Response (see Answer, page 12, para. starting on line 5)

Response to Miller "second tier" argument (page 13, para. starting on line 8)

The Examiner does not reveal or discuss what the Examiner has labeled as Appellants' "***second tier***" on page 13, paragraph starting on line 8. Instead, the Examiner merely states that "one cannot show nonobviousness by attacking references individually." Appellants respectfully submit that the Examiner is misplacing the holding of *In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981). In re Keller* holds that:

> "The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference.... Rather, the test is what the combined teachings of those references would have suggested to those of ordinary skill in the art."

However, In re Keller does not preclude an Appellant from arguing that a reference does not teach what the Examiner purports. For example, if an Applicant claims a "widget" combined with a "wadget" and the Examiner cites reference "A" as teaching a "widget" and reference "B" as teaching a "wadget", the Applicant can still argue that the Examiner erred and that reference "B" simply does not teach a "wadget" but is, instead, teaching something else. Not allowing the Appellant to refute and rebut assertions made by the Examiner regarding individual references would be tantamount to making the Examiner both judge and jury of what an individual reference actually teaches and is simply not the law under *In re Keller* nor under the MPEP.

In the instant case, Matsushita is a patent directed at a testing system for a semiconductor device and does not teach or suggest anything to do with interface controllers and their use with I/O devices. Appellants again respectfully direct the Board's attention to MPEP § 2145(X)(D)(1)

entitled "The Nature of the Teaching Is Highly Relevant." Here, Appellants simply argue that Miller does not teach or suggest what the Examiner purports Miller as teaching. Specifically, Appellants argue in the Appeal Brief that neither Matsushita nor Miller teach or suggest "selecting an interface controller from a plurality of interface controller that corresponds to the assignment request," or "associating the identified interface pins with the selected interface controller." Appellants note that the Examiner simply argues that Appellants cannot attack a reference individually (citing *In re Keller*), but does not respond or rebut Appellants contention that the cited art simply does not teach or suggest these limitations. Therefore, Appellants respectfully submit, in light of the Examiner's failure to rebut Appellants' argument, the Examiner has tacitly agreed that the references fail to teach these limitations.

Response to Miller "third tier" argument (page 13, para. starting on line 14)

Regarding Appellants "third tier" argument on Miller, the Examiner now points to columns 74-77 of Miller as allegedly teaching an "IOC assignment request." This appears to be the first time that the Examiner has cited this section of Miller as teaching an I/O controller assignment request. However, a review of this newly cited section reveals that Miller does not teach or suggest assigning an I/O controller based on an assignment request, contrary to the assertion made in the Examiner's Answer. Being an older reference, Miller teaches attaching devices to a system using a number of "channels." Each channel has a physically dedicated IOC (I/O controller). When data is transferred to a particular channel, the dedicated IOC attached to that channel handles the request. Here, instead of a processor or other logic "assigning" an IOC, the IOC requests a data transfer with the CPU and also provides the CPU with the channel number assigned to the IOC that is making the request (see Miller, abstract). Nowhere does Miller teach or suggest "*selecting a first interface controller from the plurality of interface controllers*," as claimed by Appellants. Appellants have reviewed the newly cited section (cols. 74-77) of Miller and were unable to identify any part of Miller in this section or elsewhere that teaches or suggests "selecting an interface controller from a plurality of interface controllers." Therefore, once again, the prior art (in this case Miller), simply does not teach or suggest what the Examiner purports the reference as teaching.

Conclusion

For the foregoing reasons, Appellants submit that claims 8-27 are allowable over the cited art. Accordingly, Appellants respectfully request that the Examiner's claim rejections be reversed and claims 8-27 be allowed.

Respectfully submitted,

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